UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,336	11/13/2001	Chaitanya S. Rajguru	10559-519001 / P12423	5776

20985 7590 06/04/2004

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
DESTA, ELIAS	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,336	RAJGURU, CHAITANYA S.	
	Examiner	Art Unit	
	Elias Desta	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *March 30, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *3-5,9-11,15-17 and 22-24* is/are withdrawn from consideration.

5)☒ Claim(s) *26-35* is/are allowed.

6)☒ Claim(s) *1,2,6-8,12-14, 18-21 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination

Explanation of Rejection

Claim rejection – 35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. *Claims 1, 2, 6-8, 12-14, 18-21 and 25* are rejected under 35 U.S.C. 102(b) as anticipated by *Kawahara et al.* (IEEE Journal).

In reference to claims 1, 7, 13, 19 and 20: *Kawahara et al.* teaches an apparatus for generating an internal voltage for a low voltage flash memories (see *Kawahara et al.*, Abstract). The apparatus includes:

- A charge pump having a capacity that is preset to a particular value (see *Kawahara et al.*, page 126, 1st column, paragraph 3 to 2nd column, paragraph 1, and Fig. 1).
- A measuring circuit to measure the actual capacity of the charge pumps and to reset the capacity of the charge pumps to a value based on the

measured capacity (see *Kawahara et al.*, page 129, 1st column, 1st paragraph and Fig. 1, sense and latch circuit).

- An array of memory cell because memory cells in Flash technology is set in an array arrangement (see *Kawahara et al.*, Fig. 1, memory cell).
- It is inherent that the measurement and the analysis in *Kawahara et al.* is done using a computer because in Fig. 1, the decoder is interfaced to an output port which serves for carrying out further analysis as shown in Figs. 9-11.

With regard to claims 2, 8, 14 and 21: as noted above in claims 1, 7, 13 and 20, *Kawahara et al.* further teaches that an output of the charge pump is preset to operate at a particular voltage and current (see *Kawahara et al.*, page 129, Fig. 11 and 1st column, 1st paragraph).

With regard to claims 6, 12, 18 and 25: as noted above in claims 1, 7, 13 and 19, *Kawahara et al.* further teaches that the measuring circuit includes a current sensor to sense a current at an output of the charge pump (see *Kawahara et al.*, page 129, paragraph 1 and page 130, Fig. 12).

Response to argument

3. The Examiner disagrees with the assertion that the applicant's claims are distinguishable from *Kawahara et al.*

In reference to claim 1, 7, 13, 19 and 20: as discussed in *Kawahara et al.*, Fig. 1 and page 127, paragraph 2 provides a means to measure an actual capacity of the charge pump and to reset the capacity of the charge pump to a value based on the measured capacity. Further, the system implements an accurate reference voltage, which provides a means to control the values of the charge pump capacity.

Kawahara et al. provides two charge pump voltages (VH and VP) to control the programming and erasing speed of the flash memory (see *Kawahara et al.*, page 127, 1st column and 2nd paragraph). These voltages are controlled using a reference voltage to achieve the required value (see page 127, 2nd column, 3rd paragraph). In Fig. 6(a), the charge pump is provided with a measuring circuit that enables the system to monitor the charge pump based the reference voltage because the reference voltage is connected to CR of known value. The capacitance value, as discussed in page 131, 1st column, 1st paragraph is used to reset the capacity of the charge pump to a known reference value because *Kawahara et al.* teaches that doing so guarantees the accurate control of the voltage to the charge pump.

Fig. 1 has the same high level schematic as Fig. 1 of the claimed invention, and both figures don't get into a characterization of feedback loop arrangement. However, *Kawahara et al.* uses a reference feedback mechanism to control the large and medium charge pump output to the memory cells because the voltage and temperature compensation as discussed in page 129, 1st column and 1st & 2nd paragraphs can only

achieved when the compensated values are evaluated against the output of the signals gathered at VP and VP output in order to control and improve the read and write times required by the flash memory. Further the feedback mechanism guarantees a constant current or voltage for altering the charge pump capacity.

Allowance

4. Claims 26-35 are allowed. The following is an examiner's statement of reasons for allowance:

In reference to claims 26, 30 and 35: *Kawahara et al.* does not teach resetting the nominal capacity value of the charge pump to a second capacity value based on the actual capacity and then characterizing the second value of the charge pump as sufficient capacity to simultaneously affect a second number of flash memory cells.

The remaining claims 27-29 and 31-34 are dependent upon claims 26 and 30 and contain further limitations.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Desta whose telephone number is (571)-272-2214. The examiner can normally be reached on M-Thu (8:30-7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)-272-2216. The fax

phone numbers for the organization where this application or proceeding is assigned are (703)-308-5841 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-1782.

Elias Desta
Examiner
Art Unit 2857

-ed

May 27, 2004